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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,574	KIM, HOON	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *7-12 and 17-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,13,15,16,21 and 22* is/are rejected.

7)☐ Claim(s) *2,5,6 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 01/05/2006 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 22 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claimed " step of said activation layer," is not disclosed in the application as filed. Figure 1 discloses a step in buffer layer 110, described at paragraph 0028. Figure 2 discloses a high step A1 in buffer layer 110, described at paragraph 0029. Figure 3 discloses a step A2 in buffer layer 210, described at paragraph 0036. Nowhere does Applicant describe a step formed in any of the activation layers 120, 220, shown in figures 1-3 or described in any part of the specification.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 22 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 22, line 1, "the step of said buffer layer," has no antecedent basis.

In claim 22, line 3, "the step of said activation layer," has no antecedent basis.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 1 and 13 stand rejected under 35 U.S.C. 102(b) as being anticipated by BUSTA (4,949,141).

(1) With regard to claim 1 Busta discloses a thin film transistor comprising a buffer layer 12-32 formed on a substrate 10; an 8000 angstrom thick (Note column 5 line 9. The thickness of the activation layer 34 must be known to know whether the reference meets the claims) activation layer 34 formed on said buffer layer 12-32; and a gate insulation layer 40 having a thickness of at least 1,000 angstroms (1200-2000 angstroms, see column 5 line 20) formed on said substrate 10 including said activation layer 34, with said buffer layer 12-32 having a 750 angstrom (column 5 line 9 discloses a 500-1500 angstrom range) step 32 (the size of the step is defined by projecting buffer

layer part 32. The projecting part and the step it creates will be interchangeably referred to as part "32") formed between a lower part of said activation layer 34 and a part except said lower part of said activation layer 34, said 750 angstrom step 32 being a half or less of the thickness sum (the sum of 8000, activation layer 34, and 1000, gate insulation layer 40, being 9000) of said activation layer 34 and gate insulation layer 40. Note figure 2B, column 4 lines 50-51, and column 5 lines 9,10, and 20 of Busta.

(2) With regard to claim 13 Busta discloses a thin film transistor comprising a buffer layer 12-32; an 8000 angstrom thick (Note column 5 line 9. The thickness of the activation layer 34 must be known to know whether the reference meets the claims) activation layer 34 formed on said buffer layer 12-32; and a gate insulation layer 40 having a thickness of at least 1,000 angstroms (1200-2000 angstroms, see column 5 line 20) formed on said buffer layer 12-32 and said activation layer 34, with said buffer layer 12-32 having a 750 angstrom (column 5 line 9 discloses a 500-1500 angstrom range) step 32 (the size of the step is defined by projecting buffer layer part 32. The projecting part and the step it creates will be interchangeably referred to as part "32") formed between a lower part of said activation layer 34 and a part except said lower part of said activation layer 34, and said step 32 being up to a half of the thickness sum (the sum of 8000, activation layer 34, and 1000, gate insulation layer 40, being 9000) of said activation layer 34 and gate insulation layer 40. Note figure 2B, column 4 lines 50-51, and column 5 lines 9,10, and 20 of Busta.

B. Amended claims 4 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by BUSTA (4,949,141).

(1) With regard to claim 4 Busta discloses a thin film transistor comprising a buffer layer 12-32 formed on a substrate 10; an 8500-9500 angstrom thick (8000 for layer 32, 500-1500 for polysilicon 34. Note column 5 line 9. The thickness of the activation layer 34-36 must be known to know whether the reference meets the claims) activation layer 34-36 formed on said buffer layer 12-32; and a gate insulation layer 40 having a thickness of at least 1,000 angstroms (1200-2000 angstroms, see column 5 line 20) formed on said substrate 10 including said activation layer 34-36, with said buffer layer 12-32 having a 750 angstrom (column 5 line 9 discloses a 500-1500 angstrom range) step 32 (the size of the step is defined by projecting buffer layer part 32. The projecting part and the step it creates will be interchangeably referred to as part "32") formed between a lower part of said activation layer 34-36 and a part except said lower part of said activation layer 34-36, said 750 angstrom step 32 being a half or less of the thickness sum (the sum of 8500-9500, activation layer 34-36, and 1000, gate insulation layer 40, being 9500-11000) of said activation layer 34-36 and gate insulation layer 40, said activation layer 34-36 comprising a 500 (500-1500 angstroms, note column 5 line 9) angstrom polysilicon 36. Note figure 2B, column 4 lines 50-51, and column 5 lines 9,10, and 20 of Busta.

The applicant's claim 4 does not distinguish over the Busta reference regardless of the process used to form polysilicon 36, because only the final product is relevant, not

the recited process of excimer laser annealing (ELA). See *SmithKline Beecham Corp. v. Apotex Corp.*, Fed. Cir., No. 04-1522, 2/24/06 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

(2) With regard to claim 16 Busta discloses a thin film transistor comprising a buffer layer 12-32; an 8500-9500 angstrom thick (8000 angstrom for layer 32. Note column 5 line 9. Activation layer 34-36 also comprises 500-1500 angstrom polysilicon 34. The thickness of the activation layer 34-36 must be known to know whether the reference meets the claims) activation layer 34-36 formed on said buffer layer 12-32; and a gate insulation layer 40 having a thickness of at least 1,000 angstroms (1200-2000 angstroms, see column 5 line 20) formed on said buffer layer 12-32 and said activation

layer 34-36, with said buffer layer 12-32 having a 750 angstrom (column 5 line 9 discloses a 500-1500 angstrom range) step 32 (the size of the step is defined by projecting buffer layer part 32. The projecting part and the step it creates will be interchangeably referred to as part "32") formed between a lower part of said activation layer 34-36 and a part except said lower part of said activation layer 34-36, and said step 32 being up to a half of the thickness sum of said activation layer 34-36 and gate insulation layer 40, said activation layer 34-36 comprising a 500 (500-1500 angstroms, note column 5 line 9) angstrom polysilicon 36. Note figure 2B, column 4 lines 50-51, and column 5 lines 9,10, and 20 of Busta.

The applicant's claim 16 does not distinguish over the Busta reference regardless of the process used to form polysilicon 36, because only the final product is relevant, not the recited process of excimer laser annealing (ELA).

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in

"product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

C. Claims 1 and 13 stand rejected under 35 U.S.C. 102(b) as being anticipated by ADACHI ET AL. (5,985,704).

(3) With regard to claim 1 Adachi et al. discloses a thin film transistor with a buffer layer 22 (12 in figure 1) formed on a substrate 21 (11); a 1000-1500 angstrom activation layer 13 (23 in figure 2) formed on said buffer layer 22 (12 in figure 1); and a 300 angstrom gate insulation layer 29 formed on said substrate 21 (11) including said activation layer 13 (23 in figure 2), with said buffer layer 22 (12 in figure 1) having a step "y" formed between a lower part of said activation layer 13 (23 in figure 2) and a part except said lower part of said activation layer 13 (23 in figure 2), the step "y" in the buffer layer 22 (12 in figure 1) being 80-500 angstroms thick and thus a half or less of the thickness sum (1000-1500 plus 300 angstroms) of said activation layer 23 (1000-1500 angstroms thick) and gate insulation layer 29 (300 angstroms thick). Note figures 1A-1E, 2A-E, column 4 lines 1-5 and 20-24, and column 8 lines 1-5,18-24, and 41-55 of Adachi et al.

(4) With regard to claim 13 Adachi et al. discloses a thin film transistor with a buffer layer 22 (12 in figure 1); a 1000-1500 angstrom activation layer 13 (23 in figure 2) formed on said buffer layer 22 (12 in figure 1); a 300 angstrom gate insulation layer 29 formed on said buffer layer 22 (12 in figure 1) and said activation layer 13 (23 in figure 2), with said buffer layer 22 (12 in figure 1) having a step "y" formed between a lower

part of said activation layer 13 (23 in figure 2) and a part except said lower part of said activation layer 13 (23 in figure 2), said step "y" being 80-500 angstroms thick and thus up to a half of the thickness sum (1000-1500 plus 30-300 angstroms) of said activation layer 23 (1000-1500 angstroms thick) and gate insulation layer 29 (30-300 angstroms thick). Note figures 1A-1E, 2A-E, column 4 lines 1-5 and 20-24, and column 8 lines 1-5,18-24, and 41-55 of Adachi et al.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Amended claims 3 and 15, and new claim 21, are rejected under 35 U.S.C. 103(a) as being unpatentable over ADACHI ET AL. (5,985,704) in view of YAMAZAKI ET AL. (2004/0211356).

Adachi et al. discloses a thin film transistor with all the limitations of claims 3,15, and 21, including that the step be 350 angstroms (Adachi et al. disclose 80-500 angstroms) in the activation layer, except that the thickness of the gate insulation layer be at least 400 (400 angstroms or more) angstroms and that the activation layer comprise a polysilicon having a thickness of 300 angstroms. Note figures 1A-1E, 2A-E, column 4 lines 1-5 and 20-24, and column 8 lines 1-5,18-24, and 41-55 of Adachi et al.

However, Yamazaki et al. discloses a thin film transistor with that a thickness of a gate insulation layer 405 that is 400 angstroms or more (1000-1500 angstroms) and an activation layer 403 comprising KrF excimer laser activated polysilicon having a thickness of 300 angstroms. Note figures 7A-D, 10A-C, and paragraphs 0088-0098 of Yamazaki et al. Therefore, it would have been obvious to a person having skill in the art to modify the dimensions of the of Adachi et al.'s thin film transistor to the dimensions taught by Yamazaki et al. in order to increase gate-channel breakdown voltage by thickening the gate insulating film, while at the same time making it easier to fully deplete the channel, by making the channel shallower, to thus provide a TFT able to perform over a wider range of voltages.

The applicant's claims 3 and 15 do not distinguish over the Adachi et al. or Yamazaki et al. references regardless of the process used to form the activation layer, because only the final product is relevant, not the recited process of solid phase crystallization. See *SmithKline Beecham Corp. v. Apotex Corp.*, Fed. Cir., No. 04-1522, 2/24/06 ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it

is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Allowable Subject Matter

6. Claims 2,5,6, and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 3,4, 15, and 16 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues, see pages 13-14 of the remarks, that "Concerning claims 2 and 14, Busta fails to disclose the buffer layer having a step to such a degree that the thickness of the gate insulation layer in not changed or even [Sic. Applicant apparent refers to the claim language "is not changed on said side wall of said buffer layer."] on the sidewall of the buffer layer. There must be an actual disclosure in Busta concerning the unchanged thickness of the gate insulation as related to the step in the buffer layer... the Examiner cannot rely on the drawings to show the unchanged thickness as

there is no related disclosure in the specification indicating such. Specifically MPEP 2125 ... states ... 'When the reference does not disclose that the drawings are to scale and is silent as to dimensions, arguments based on measurement of the drawing features are of little value.'" On page 16 Applicant similarly argues that only in not-to-scale drawings does Adachi et al. show that the thickness of the gate insulation layer is not changed on the sidewall of the buffer layer. Applicant's arguments have been fully considered and are persuasive. The 102(b) rejections of claims 2,5,6, and 14 have been withdrawn.

Applicant's arguments with regard to claims 1 and 13 have been fully considered but they are not persuasive.

It is argued, at page 12 of the remarks, that "concerning claims 1 and 13, reference 32 is clearly not the buffer layer as claimed in the present invention. Claim 1 states that the buffer layer is formed on a substrate with a separate activation layer formed on the buffer layer." Applicant misstates the examiner's position, which is a waste of both the applicant's and the examiner's time. As clearly stated above, Busta's layers 12 and 32 together form the claimed buffer layer, with substrate 10 below, and activation layer 34 above.

It is further argued at page 12 that "Reference 12 is stated clearly in Busta as being a pixel element and reference 32 is clearly the drain layer, therefore, neither reference 12 or 32 is the buffer layer." However, Busta discloses a laminate layer 12-32 that meets all of the limitations the claims require of the buffer layer. The fact that Busta

chooses to use different language to describe this layer has no legal or practical significance.

It is argued, at page 13 of the remarks, that "The present invention claims the buffer layer having a step formed, and not a pixel layer having a drain 32 which is being construed as a buffer layer." These remarks contribute nothing useful. If applicant's claims happen to read on a device applicant does not consider to be part of applicant's invention, applicant is free to amend his claims.

It is argued, at page 14 of the remarks, that "Concerning claims 4, 6, 16, the thickness of the activation layer being 500 Angstroms and the step being 750 Angstroms and the gate insulation layer being at least 1000 Angstroms is not disclosed since layer 34, which the Examiner states is the activation layer is disclosed to be 8000-15000 Angstroms. 500 Angstroms is not within the range of 8000-15000." Because claims 4 and 16 have been amended this argument no longer makes any sense. Claims 4 and 16 require the "polysilicon" (Busta's part 36) to be 500 Angstroms thick. Claims 4, 6, and 16 don't require the "activation layer" (Busta's part 34) to be of any specific thickness.

It is further argued, at page 14 of the remarks, that "Concerning claims 4, 6 and 16, there is no disclosure in Busta that there is a step of 350 Angstroms in the activation layer." However, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., activation layer comprises a step) are not recited in the rejected

claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). As noted above, the claims do not recite a step in the activation layer, and further, the only step disclosed in the application as filed is formed in the buffer layer.

It is argued, at page 15 of the remarks, that "Concerning claims 1 and 13, the Examiner has stated that it is only the final product that is important in the claim and yet, the Examiner refers to layers in the interim process." However, the Examiner's statement ("only the final product is relevant, not the recited process of excimer laser annealing") concerned only the claims with elements (polysilicons) having product-by-process limitations. Applicant's argument lacks relevancy in a discussion of claims 1 and 13.

It is argued, at page 16 of the remarks, that "the Examiner states that gate insulation layer is 300 Angstroms. However, no such disclosure is ever given in Adachi. Adachi only refers to a gate insulation layer 29 and that is all."

This last statement is simply false. Did Applicant know it was false when he advanced it as grounds for the patentability of his claims? It seems overwhelmingly likely Applicant knew that column 8 lines 50-52 of Adachi et al. read,

> "Also, in accordance with another aspect the invention, a gate insulating layer can be formed by forming a thin oxide layer (30-300Å) by the thermal oxidation or light oxidation."

These three lines were three of only thirty-seven lines, total, that the Examiner pin-cited for Applicant's attention in the last Action. Why does Applicant believe that Applicant can gain an enforceable patent by putting false statements on the record?

With regard to the 35 USC § 103 rejection of claims 3,5, and 15 over ADACHI ET AL. in view of YAMAZAKI ET AL. it is argued at page 19 of the remarks, that "Further, the Examiner states that the polysilicon of the activation layer is 300 Angstroms is taught in Adachi. [Sic.] However, a search of Adachi shows no such disclosure relating to 300 Angstroms of the polysilicon of the activation layer." The examiner's exact words were "Adachi et al. discloses a thin film transistor with all the limitations of claims 3,15, and 21, including that the step be 350 angstroms (Adachi et al. disclose 80-500 angstroms) in the activation layer, except that the thickness of the gate insulation layer be at least 400 (400 angstroms or more) angstroms and that the activation layer comprise a polysilicon having a thickness of 300 angstroms." (Emphasis added). Why is Applicant so willing to misrepresent the Examiner's statements?

With further regard to the 35 USC § 103 rejection of claims 3,5, and 15 over ADACHI ET AL. in view of YAMAZAKI ET AL. it is argued at page 19 of the remarks that "The Examiner further states that yet applicant's claims 4, 6, and 16 require a 750-angstrom step. The Examiner states that to accomplish such a very extreme step, it is safer to build a vertical TFT, such as taught by Busta, where the gate, and the gate insulator, is essentially laid down on the side of the step. However, the Examiner's

argument above is showing that the references are teaching away from the present invention and therefore, should not be combined."

The phrase "the present invention," is completely meaningless as far as the Examiner is concerned. All that is relevant to the Examiner's task is the claimed invention, claim after claim after claim, one claim at a time. If applicant chooses to claim an invention in claims 3,5, and 15 that is incompatible with the invention Applicant claims in claims 4,6, and 16 this is Applicant's privilege, and simply results in the Examiner's having to perform two separate searches, one to find art (BUSTA) for claims 4,6, and 16, and a second search to find art (ADACHI ET AL. in view of YAMAZAKI ET AL.) for claims 3,5, and 15. It is true that the combined teachings of ADACHI ET AL. and YAMAZAKI ET AL. "teach away" from claims 4,6, and 16. This is why claims 4,6, and 16 are rejected over BUSTA. ADACHI ET AL. and YAMAZAKI ET AL combine to teach the invention claimed in claims 3,5, and 15. The combined teachings of ADACHI ET AL. and YAMAZAKI ET AL. do not "teach away" from "the present invention" recited in claims 3,5, and 15.

It is argued, at page 19 of the remarks, that "The Examiner states that the motivation to combine the references is to increase gate-channel breakdown voltage by thickening the gate insulating film, while at the same time making it easier to fully deplete the channel, by making the channel shallower, to thus provide a TFT able to perform over a wider range of voltages. However, this does not relate to the inclusion of the thickness of the gate insulation layer specifically."

Again, Applicant gives the appearance of deliberately attempting to distort the truth for Applicant's own benefit. The examiner stated that increasing the gate insulating film from the relatively thin gate insulating film thickness (30-300 angstroms, note, again, column 8 lines 50-52 of Adachi et al.) disclosed by Adachi et al. to the slightly thicker (400 angstrom) gate insulating film thickness disclosed by Yamazaki et al. would increase the gate-channel breakdown voltage. Relating the thickness of the gate insulating film to a beneficial increase in gate-channel breakdown voltage is a textbook example of "relat[ing] to the inclusion of the thickness of the gate insulation layer specifically," as Applicant so eloquently states the requirement of a showing of some suggestion or motivation to make the modification disclosed by the combined references.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
03/06